We claim:

1. In a process for forming dual gate oxides for use in high performance DRAM systems or logic circuits, the improvement comprising using a "shadow effect" to control gate oxide thickness at active area (AA) corners adjacent a shallow trench isolation (STI) region, comprising:

I) a. forming an active area by depositing over a semiconductor substrate, a patterned hard mask nitride layer exposing portions of said substrate so as to define an isolation region;

b. etching exposed regions of said substrate using said patterned hard mask layer to form an isolation trench in the isolation region;

c. oxidizing said substrate to form a thermal oxide layer in the isolation trench and the capacitor trench;

d. depositing an oxide layer over the thermal oxide layer to fill unfilled portions of the isolation trench;

e. removing said patterned hard mask;

f. planarizing said substrate and forming a pad nitride strip;

II) forming a sacrificial gate oxide layer in the areas of the semiconductor substrate surface where the pad nitride has been stripped off;

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III) affecting channel implants in selected areas using resist masks;

IV) affecting a first low dose angled nitrogen implant without using an implant mask in a manner to limit the nitrogen dose in the active area to the inner part of the gate area so that the angled nitrogen dose in the Shadow part" of the active area is less than the amount of the nitrogen dose implanted in the remaining non-shadowed area to cause spatial thickness distribution of all exposed oxide areas.

V) affecting masking so that nitrogen ions (N_2^+) to be implanted do not penetrate the masked region; and

VI) affecting a second nitrogen ion implantation by employing a "shadow effect" inducing means at a temperature sufficient to provide a lesser amount of nitrogen ion dosage in the inner part of the gate area so that the angled nitrogen in the "shadow part" part of the active area is less than the amount of nitrogen dose implanted in the remaining non-shadowed area.

2. The process of claim 1 wherein said "shadow effect" inducing means is by angled nitrogen ion implantation at an angle either greater or less than 90° with respect to the surface normal of said semiconductor or wafer substrate.

3. The process of claim 1 wherein said 'shadow effect" inducing means in step VI is by nitride spacers followed by vertical or 90° nitrogen ion implantation.

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4. The process of claim 2 wherein said oxidation is performed at about 900°C under dry conditions .

5. The process of claim 2 wherein said oxidation is performed at about 800°C under a combination of dry and wet oxidation conditions.

6. The process of claim 3 wherein said oxidation is preformed at about 900°C under dry conditions.

7. The process of claim 3 wherein said oxidation is performed at about 800°C under a combination of dry and wet oxidation conditions.

8. The process of claim 3 wherein said nitride is silicon nitride.

9. The process of claim 3 wherein between said nitride spacers and vertical nitrogen implantation, steam oxidation is employed to convert said nitride to an oxide.

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